WHAT IS CLAIMED IS:

1. A method for implementing communication between data processors, comprising:

a first task running on a first data processor determining that communication is desired between the first task and a second task running on a second data processor;

the first data processor determining whether the second task is blocked with respect to communication on a predetermined communication channel;

if the second task is blocked with respect to communication on the predetermined communication channel, the first data processor interrupting the second data processor to inform the second data processor of the desired communication and thereafter participating in the desired communication on the predetermined communication channel; and

if the second task is not blocked with respect to communication on the predetermined communication channel, the first data processor participating in the desired communication on the predetermined communication channel without interrupting the second data processor.

2. The method of Claim 1, including, if the second task is blocked with respect to communication on the predetermined communication channel, the first data processor providing in a memory shared by the first and second data processors an

indication that the second data processor is not blocked with respect to communication on the predetermined communication channel.

3. The method of Claim 1, wherein said determining step includes the first data processor accessing a memory that is shared by the first and second data processors.

4. The method of Claim 3, wherein said determining step includes the first data processor obtaining exclusive access to the shared memory.

5. The method of Claim 4, wherein said determining step includes the first data processor retrieving from the shared memory information indicative of whether the second task is blocked with respect to communication on the predetermined communication channel.

6. The method of Claim 1, wherein said performing step includes the first task exchanging data buffer attributes with the second task.

7. The method of Claim 6, wherein said performing step includes the first task swapping buffer data and buffer attributes with the second task.

8. The method of Claim 6, wherein said performing step includes the first task copying from data buffers data provided by the second task, and the first task copying attributes associated with said data buffers.

9. The method of Claim 1, including, after said performing step, the first data processor blocking the first task with respect to communication on said predetermined communication channel and providing in a memory shared by the first and second data processors an indication that the first task is blocked with respect to communication on the predetermined communication channel.

10. The method of Claim 9, including the second data processor interrupting the first data processor to indicate that communication is desired between the second task and the first task, and the first data processor unblocking the first task for communication on the predetermined communication channel in response to said interrupting step.

11. The method of Claim 10, including the second data processor, in conjunction with said interrupting step, providing in a memory shared by the first and second data processors an indication that the first data processor is not blocked with respect to communication on the predetermined communication channel.

12. The method of Claim 2, including the second data processor unblocking the second task with respect to communication on the predetermined communication channel in response to said interrupting step.

13. A data processing system, comprising:

a first data processor;

a second data processor coupled to said first data processor for permitting communication therebetween;

said first data processor including a device driver for implementing a desired communication between a first task running on said first data processor and a second task running on said second data processor;

a communication port coupled to said device driver for permitting said device driver to access a communication channel for the desired communication, said communication port further for permitting said device driver to receive information indicative of whether the second task is blocked with respect to communication on said communication channel; and

said device driver including logic responsive to a blocked indication for outputting to said second data processor via said communication port an interrupt signal to inform said second data processor of the desired communication, said logic responsive to an indication that the further task is not blocked for permitting said device driver to

participate in the desired communication on said communication channel without outputting said interrupt signal to said second data processor.

14. The system of Claim 13, wherein said communication channel includes a memory apparatus shared by said first and second data processors.

15. The system of Claim 14, wherein said shared memory apparatus includes said information indicative of whether said second task is blocked, said communication port of said first data processor coupled to said shared memory apparatus for permitting said device driver of said first data processor to access said information indicative of whether said second task is blocked.

16. The system of Claim 15, including a memory access apparatus coupled between said shared memory apparatus and said first and second data processors, said memory access apparatus responsive to signaling from said first data processor for permitting said device driver of said first data processor to access said shared memory while simultaneously excluding said second data processor from accessing said shared memory.

17. The system of Claim 13, wherein said first data processor includes a scheduler for selectively blocking and unblocking said first task with respect to

communication on said communication channel, said device driver coupled to said scheduler and operable after performing the desired communication for signaling said scheduler to block said first task with respect to communication on said communication channel, and wherein said communication channel includes a memory apparatus shared by said first and second data processors, said device driver further operable after performing the desired communication for storing in said shared memory apparatus an indication that said first task is blocked with respect to communication on said communication channel.

18. The system of Claim 17, wherein said communication port of said first data processor is coupled to said second data processor for receiving therefrom an interrupt signal, said device driver of said first data processor responsive to said interrupt signal for signaling said scheduler to unblock said first task.

19. The system of Claim 13, including a memory apparatus coupled to said first and second data processors, said device driver of said first data processor responsive to said blocked indication for providing within said memory apparatus an indication that said second task is not blocked with respect to communication on said communication channel.

20. The system of Claim 19, wherein said second data processor is coupled to said communication port of said first data processor for providing an interrupt signal to said device driver, said second data processor operable in conjunction with providing said interrupt signal to said device driver for also providing in said memory apparatus an indication that said first task is not blocked with respect to communication on said communication channel.

21. The system of Claim 20, wherein said first data processor includes a scheduler for selectively blocking and unblocking said first task with respect to communication on said communication channel, said device driver coupled to said scheduler and responsive to said interrupt signal for signaling said scheduler to unblock said first task with respect to communication on said communication channel.

22. The system of Claim 21, including a memory access apparatus coupled to said memory apparatus and said first and second data processors, said memory access apparatus responsive to signaling from said first data processor for permitting said first data processor to access said memory apparatus while simultaneously preventing said second data processor from accessing said memory apparatus, and said memory access apparatus responsive to signaling from said second data processor for permitting said second data processor to access said memory apparatus while simultaneously preventing said first data processor from accessing said memory apparatus.

23. The system of Claim 22, wherein said memory access apparatus includes a data switch.

24. The system of Claim 22, provided on a single integrated circuit chip.

25. The system of Claim 24, including a man/machine interface coupled to said first data processor for permitting communication between said first data processor and a user.

26. The system of Claim 13, provided on a single integrated circuit chip.

27. The system of Claim 13, including a man/machine interface coupled to said first data processor for permitting communication between said first data processor and a user.

28. The system of Claim 13, wherein said first data processor is a microprocessor and said second data processor is a digital signal processor.

29. A data processing apparatus, comprising:

a device driver for implementing a desired communication between a task running on the data processing apparatus and a further task running on a further data processing apparatus;

a communication port coupled to said device driver for permitting said device driver to access a communication channel on which the desired communication can occur, said communication port further for permitting said device driver to receive information indicative of whether the further task is blocked with respect to communication on said communication channel; and

said device driver including logic responsive to a blocked indication for outputting to the further data processing apparatus an interrupt signal to inform the further data processing apparatus of the desired communication, said logic responsive to an indication that the further task is not blocked for permitting said device driver to participate in the desired communication on said communication channel without outputting said interrupt signal to the further data processing apparatus.

30. The apparatus of Claim 29, including a scheduler for selectively blocking and unblocking said first-mentioned task with respect to communication on said communication channel, said device driver coupled to said scheduler and operable after performing the desired communication for signaling said scheduler to block said first-mentioned task with respect to communication on said communication channel.

31. The apparatus of Claim 29, wherein said communication port is further for receiving an interrupt signal from the further data processing apparatus, said device driver responsive to said interrupt signal for signaling said scheduler to unblock said first-mentioned task with respect to communication on said communication channel.